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Single-Ended HEMT Multiplier Design Using Reflector Networks

Donald G. Thomas, Jr. and G. R. Branner

***Abstract*—Microwave and RF frequency multipliers are employed in a large number of communications, radar, civilian, and military systems. This paper presents the development of active doublers operating in S and C frequency bands. These devices are unique in that high electron-mobility transistors (Fujitsu FHX35LG) are employed in an unbalanced configuration utilizing "reflector" networks simultaneously on the input and output to reflect the second harmonic signal into the gate of the device and the fundamental signal into the drain simultaneously at appropriate phase angles to optimize performance. Measured and simulated results are presented on over 20 multiplier designs to verify the design philosophy. Conversion gains of approximately 7 dB are presented for narrow-band designs (5% bandwidth), 5 dB for medium-bandwidth designs (15%), and 4 dB for wide-bandwidth designs (35%). The fundamental and third harmonic rejection is approximately 40 dBc for the narrow-band designs and greater than 50 dBc for the medium and wide-band designs.**

I. Introduction

Numerous techniques exist for realization of frequency multipliers using passive or active devices. While high electron-mobility transistors (HEMTs) are traditionally employed in high-gain or low-noise amplifiers, less information is available on their use in multiplier applications. This is in marked contrast with multiplier realizations employing bipolar and FET devices.

The basic configuration of Fig. 1 is employed in the frequency multiplier realization of this paper. The input network is designed to pass the fundamental frequency component to the gate of the HEMT (common-source configuration), while suppressing higher harmonic components. Likewise, the output network suppresses the fundamental and other undesired harmonics, while passing the desired harmonic. The frequency multiplier reflector network design philosophy implemented in this paper is applied to frequency doublers utilizing a fundamental frequency of 3 GHz as a vehicle.

As mentioned previously, a primary objective of the output and input networks is to suppress the fundamental and second harmonics, respectively. In the process of suppressing the undesired signals, it appears that not a great amount of attention has been focused on the concept of reflecting signals back into the device from the input and output networks, although it has been utilized occasionally as pointed out below. The device nonlinearities cause harmonics and the fundamental to mix with other frequency components and either enhance or degrade the signal at the desired output harmonic. Therefore, it is important for the reflected signal to be phased properly to interfere constructively with the desired harmonic. Thus, in concert with their primary filtering and matching functions, the input and output networks of Fig. 1 can be designed in such a way that they are reflector networks meeting the above criteria.

Due to the complexity of calculating the actual effects of the reflector networks, the published literature to date on this topic is sparse [1]–[4]. Using reflector networks as a design tool for frequency doublers, Hirota [1] gave simulated data on the effects of a reflector network on the output of a GaAsFET versus conversion gain, and realized

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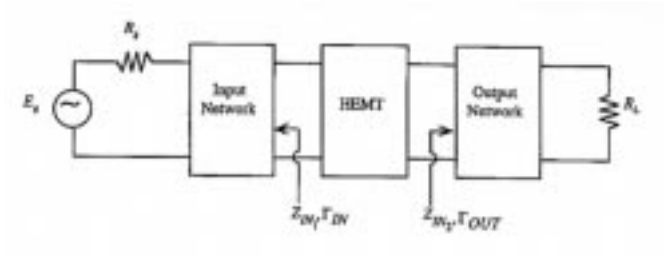

Fig. 1. Network configuration model.

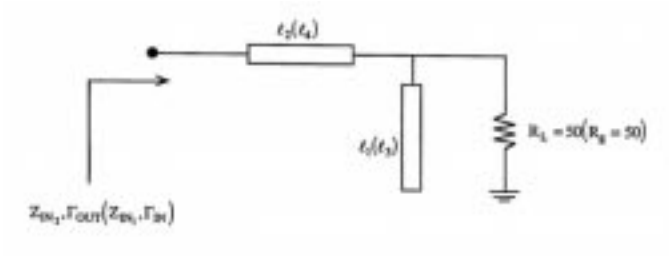

Fig. 2. Fundamental output (input) reflector network.

a narrow-band conversion gain of 2.9 dB. Borg [2] and Rauscher [3] showed that there is an advantage in using a reflector circuit on the output. Rauscher[1] primarily used simulated data without experimental data to verify the accuracy of the computer simulations. In the final multiplier design, the multiplier possessed less than 0 dB of conversion gain after requiring tuning. Based on an examination of the literature, there does not appear to be a significant amount of multiplier design incorporating reflector networks, especially on both input and output ports simultaneously. Additionally, very little, if any, reflector-based work provides both highly accurate modeled and measured data.

The multiplier realizations presented in this paper are unique in that the analysis quantitatively assesses the effect of reflector networks on both input and output ports simultaneously and is performed on HEMT[2] transistors. Measured and modeled data are presented throughout the analytical process to validate the results. A number of designs are presented, which produce high conversion gains, narrow, medium, and wide bandwidths, and operate with low dc power consumption due to HEMT biasing at pinchoff ($V_{\rm gs} = V_p$). Furthermore, in contrast with previous results, alternate designs for reflector networks for HEMT multipliers are also discussed, employed, and experimentally verified.

II. Analysis of Reflector Network Effects Consideration of Reflection Phase Angle

As mentioned above, for optimization of conversion gain, the input and output networks depicted in Fig. 1 are designed such that they are reflector networks in addition to their primary functions of filtering and matching. These reflector networks are utilized below in the synthesis of frequency doublers operating at a fundamental frequency of 3 GHz. As alluded to previously, the input network of Fig. 1 should be designed such that it reflects the second harmonic component back into the gate at the proper phase angle to interfere constructively for optimum conversion gain. Similarly, the output network is designed such that it reflects the fundamental signal properly phased into the drain of the HEMT.

Fig. 2 shows a fundamental reflector network topology, which may be employed for output and input networks (Fig. 1). In results presented below, ℓ_1, ℓ_2, $Z_{\rm IN_2}$, $\Gamma_{\rm OUT}$, and R_L are employed to describe the output reflector network, while the parameters in parenthesis (ℓ_3, ℓ_4, $Z_{\rm IN_1}$, $\Gamma_{\rm IN}$, and R_g) describe the input reflector network as viewed from the gate. That these networks do, in fact, provide the requisite reflection at $f_{\rm o}$ and $2f_{\rm o}$ for output and input can be seen from computation of $\Gamma_{\rm OUT}$ and $\Gamma_{\rm IN}$, respectively, as ℓ_2 and ℓ_4 are varied over the ranges of interest.

In concert with the aforementioned objectives, with $\lambda_{f_{\rm o}}$ equal to the wavelength at the fundamental frequency, ℓ_1 equals a quarter-wavelength ($\ell_1 = \lambda_{f_{\rm o}}/4$) and ℓ_2 is nominally a half-wavelength ($\ell_2 = \lambda_{f_{\rm o}}/2$) at the fundamental frequency ($f_{\rm o}$) for the output reflector network. Similarly, with $\lambda_{2f_{\rm o}}$ equal to the wavelength at the second harmonic, ℓ_3 and ℓ_4 are a quarter-wavelength ($\ell_3 = \lambda_{2f_{\rm o}}/4$) and nominally a half-wavelength ($\ell_4 = \lambda_{2f_{\rm o}}/2$), respectively, at $2f_{\rm o}$.

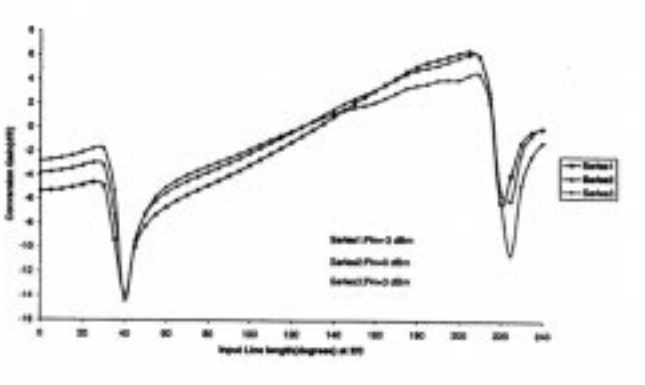

Fig. 3. Simulated conversion gain of frequency doubler versus input transmission line length (ℓ_4) at the second harmonic ($V_{\rm gs} = -0.6$ V, $V_{\rm ds} = 3$ V).

A. Effect of Reflection Phase Angle on Conversion Gain

Although more exotic reflector networks will be subsequently introduced, initial observations are developed utilizing the circuits depicted in Fig. 2. Initially, optimum narrow-band conversion gains will be illustrated by optimizing the phase angles of $\Gamma_{\rm IN}$ and $\Gamma_{\rm OUT}$ via ℓ_4 and ℓ_2, respectively. The HEMT employed is the Fujitsu FHX 35 LG and its computer model can be obtained from [5]. Furthermore, comparisons between the computer model and measured device data can be observed in [6, Fig. 2].

With the parameters of the fundamental output network constrained to the aforementioned nominal values, Fig. 3[3] shows the effect of varying ℓ_4 of the fundamental input reflector network over a range from 0° to 240° (at $2f_{\rm o}$) for three different input powers (-3, 0, and $+3$ dBm). These results quantitatively illustrate the effect of stub location on conversion gain for second harmonic energy reflection at the gate.

The maximum conversion gain is seen to occur at $\ell_4 \approx 200^\circ$ at $2f_{\rm o}$, and it may also be observed that the conversion gain variation may be as great as 20 dB over this range of ℓ_4. Fig. 4 presents analogous data for variation of ℓ_2 (fundamental output reflector network) from 0 to $\lambda_{f_{\rm o}}/2 (180^\circ$ at $f_{\rm o})$, $\ell_1 = \lambda_{f_{\rm o}/4}$ while simultaneously utilizing the nominal input reflector network $\ell_3 = \lambda_{2f_{\rm o}}/4$, $\ell_4 = \lambda_{2f_{\rm o}}/2$. These results demonstrate that there is as much as a 27-dB variation in

[1]Also provides analysis data for an input reflector.

[2]The Fujitsu FHX 35 LG HEMT transistor is employed in this paper. Its computer model can be accessed from the HP EESOF LIBRA Device Model Library [5],[6, Fig. 2].

[3]All results in the remaining figures have the HEMT biased with $V_{\rm gs} = -0.6$ V, $V_{\rm ds} = 3$ V and $P_{\rm IN} = 0$ dBm unless otherwise specified

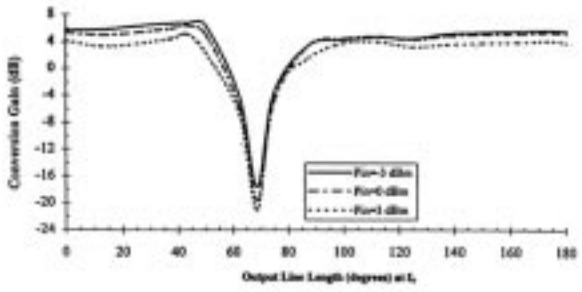

Fig. 4. Simulated conversion gain of frequency doubler versus output transmission line length (ℓ_2) at $f_o(V_{gs} = -0.6$ V, $V_{ds} = 3$ V).

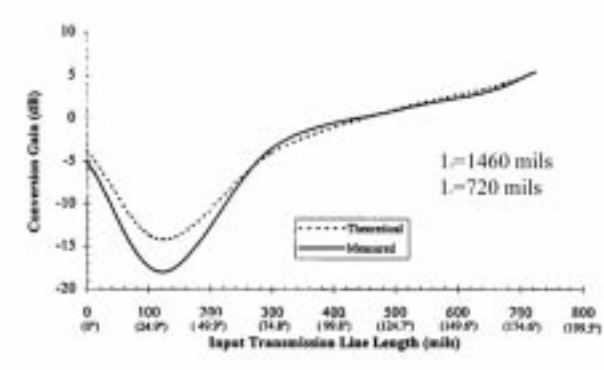

Fig. 5. Conversion gain of HEMT doubler versus input transmission line length (ℓ_4) at $2f_o(P_{in} = 0$ dBm, $V_{gs} = -0.6$ V, $V_{ds} = 3$ V).

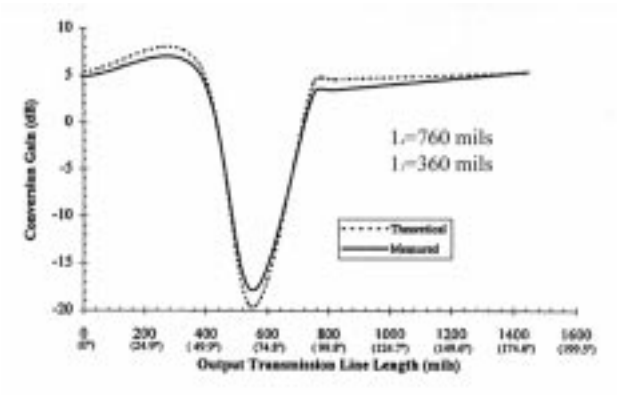

Fig. 6. Conversion gain of HEMT doubler versus output transmission-line length (ℓ_2) at $f_o(P_{in} = 0$ dBm, $V_{gs} = -0.6$ V, $V_{ds} = 3$ V).

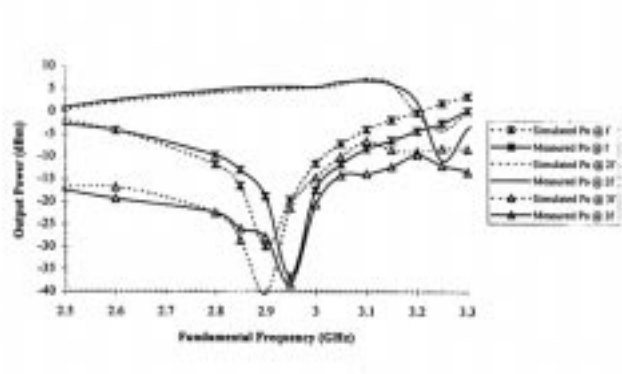

Fig. 7. Narrow-band HEMT doubler design.

conversion gain and that the optimal length for ℓ_2 is $\approx 44^\circ$ to realize maximum conversion gain.

The efficacy of the previous models in generating accurate results has been authenticated by the development of in-depth experimental data. Toward this end, a series of 16 distinct multipliers were designed, constructed, and tested. The passive circuits utilized sections of 50-Ω line realized in 20-mil Duroid, copper thickness 1.5 mil, linewidths realized measured at $\approx$60 mil, $\varepsilon_r \cong 2.17$.

The first series of experimental designs (eight distinct circuits of varying values of ℓ_4) authenticated the predicted results of Fig. 3 for the input reflector network. The comparative results are presented in Fig. 5 as conversion gain versus ℓ_4. The responses are seen to agree exceptionally well for lengths beyond 50° ($\Delta \leq 2$ dB), and for values below 50°, they follow the response trend with a worst-case difference of 5 dB. *Realized* dimensions are presented in Figs. 5 and 6.

The second series repeated the above experimental process duplicating the conditions of Fig. 4 ($0 \leq \ell_2 \leq \lambda_{f_o}/2$) with eight distinct output networks. Simulated and measured results compare very favorably over the entire range of ℓ_2 values (Fig. 6). These results (Figs. 5 and 6) provide the following two significant conclusions: 1) measured and modeled results agree quite closely, and this provides confidence in predictive conclusions in the ensuing HEMT-based designs and 2) requisite line lengths and reflection angles providing optimum conversion gains can easily be extracted from the data.

III. Circuit Design

A. Narrow-Band Doubler Design

Synthesis of a narrow-band HEMT doubler utilizes the fundamental input and output reflector networks (Fig. 2) as a basis in conjunction with the results of Figs. 3 and 5. A simulation of this circuit topology provides a prediction of a center-band conversion gain of $\approx$7 dB, given the respective electrical lengths of ℓ_4 and ℓ_2 of 180° at f_o and $2f_o$, respectively.

The measured and simulated performance of this multiplier realization are presented in Fig. 7. A perusal of this figure reveals that the measured conversion gain is $\approx$6 dB, that fundamental and third order suppression are greater than 40 dBc at a fundamental frequency of 2.95 GHz, and that measured and simulated results are in agreement. The narrow-band response (typically 5%–10%) of this design is an outcome of the application of single stub input and output reflector realizations.

An alternative narrow-band design creates more rolloff of the conversion gain response by synthesizing an output reflector network consisting of a length of transmission line cascaded with a bandpass filter structure. In this realization, the length of the cascaded transmission line is adjusted to provide the proper output reflector network phase angle for optimum conversion gain ($\approx 44^\circ$ and a corresponding theoretical coefficient angle of $\approx 93^\circ$ at the fundamental frequency, as shown in Figs. 4 and 6). This presents the correct impedance to resonate the drain reactance of the HEMT at the fundamental frequency. The input reflector network is the same as the previous case ($\ell_4 = \lambda_{2f_0}/2$ and $\ell_3 = \lambda_{2f_0}/4$).

Two separate designs incorporated, respectively, one- and two-section filters for the bandpass structures. Fig. 8 shows the performance of the one-section design (6-dB conversion gain, greater harmonic suppression $\geq$25 dBc over a wider band due to filter action). The second (two-section) design (Fig. 9) provides 4.5-dB conversion gain and greatly improved harmonic suppression (≈ -50 dBc).

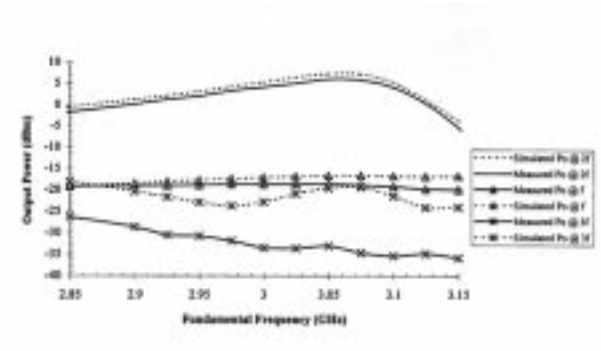

Fig. 8. Narrow-band HEMT doubler design with one section filter.

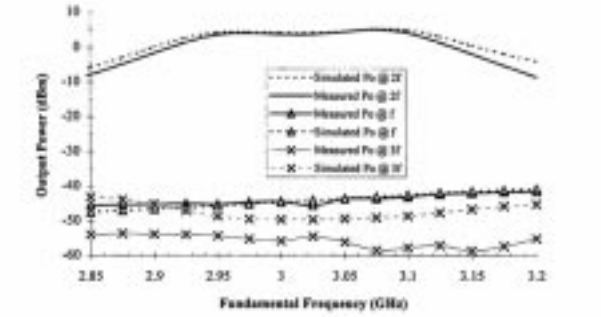

Fig. 9. Narrow-band HEMT doubler design with two section filter.

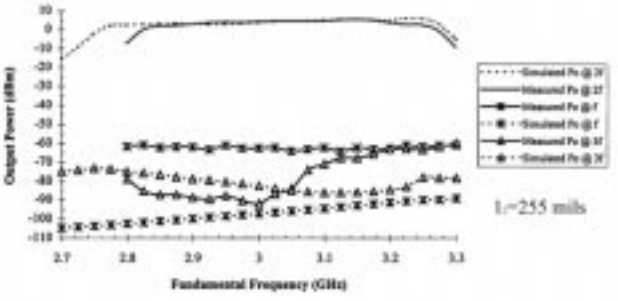

Fig. 10. Medium-band HEMT doubler design.

B. Wider Bandwidth Designs

Broader bandwidth HEMT multiplier conversion gain and harmonic suppression can be achieved by employing wider band reflector network responses. In particular, it is shown below that by extending the bandwidths of the output reflector network, significantly wider doubler frequency performance is achieved.

Synthesis of a medium-band HEMT multiplier realization is illustrated utilizing a HEMT/series transmission line for $\ell_2/$ bandpass filter cascade. The output reflector network employs a 15% edge-coupled bandpass filter and the input reflector network is the nominal design discussed earlier ($\ell_4 = \lambda_{2f_0}/2$ and $\ell_3 = \lambda_{2f_0}/4$) As in previous designs, the cascaded transmission line provides the proper reflection phase angle of the fundamental frequency at the output. Fig. 10 is a plot of measured and modeled gain responses for second, fundamental, and third harmonic signals emerging from the HEMT multiplier. A perusal of this figure reveals doubler conversion gains of 4 dB$\pm$1 dB have been achieved with a 3-dB bandwidth of 15%. Furthermore, fundamental and third harmonic suppression is observed to be greater than 65 dBc.

Wider band designs are synthesized by extension of the concept utilized for medium-band responses. In this case, the filter employed in the output reflector cascade is a 45% fifth-order realization [7] and the input reflector is the nominal realization used previously. The measured and modeled responses in Fig. 11 demonstrate extended conversion gain bandwidth performance and excellent harmonic suppression. This figure demonstrates conversion gain of 3 dB$\pm$1 dB, 3-dB bandwidth of 35%, and fundamental and third harmonic frequency suppression of greater than 45 dBc.

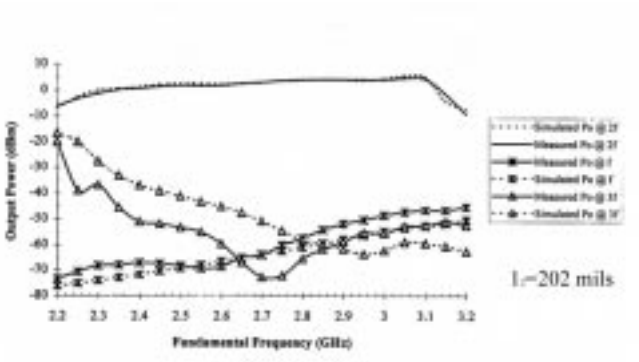

Fig. 11. Wide-band HEMT doubler design.

IV. Conclusion

This paper has presented techniques for synthesis of active single-ended frequency doublers employing HEMT transistors. These techniques incorporate reflector networks for providing excellent performance characteristics, which include efficient conversion gain and harmonic suppression. This performance is demonstrated quantitatively by both computer simulations and corresponding measured results. These results quantitatively illustrate the improvement in conversion gain using reflector networks on the input and output with proper phase angles to obtain optimum performance. These single-ended designs are useful for narrow- and wide-bandwidth applications. Since networks employing single stubs limit the operational bandwidth, incorporating filters into the designs provides bandwidth extension and improves the harmonic suppression. Of course, this improvement in bandwidth and harmonic suppression comes at the expense of the conversion gain. Another advantage of these designs is that they are single ended. This condition alleviates the necessity for complex baluns or transformers.

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